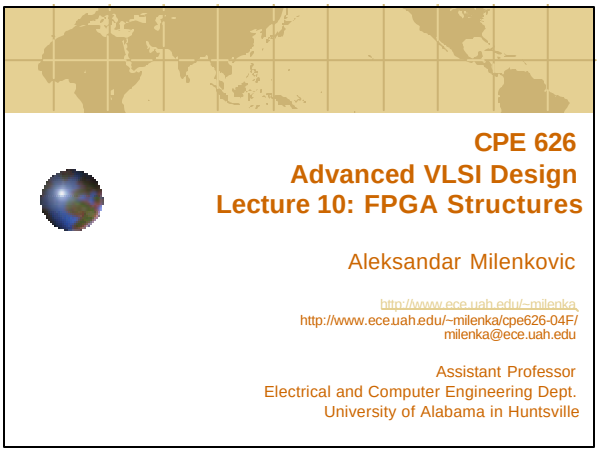

CPE 626
Advanced VLSI Design
Lecture 10: FPGA Structures

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Outline

Programmable ASICs

- Introduction
- Antifuse
- Static RAM
- EPROM, EEPROM Technology

Introduction

- Programmable ASICs
  - PLDs – Programmable Logic Devices
    - started as small devices (to replace a handful of TTLs)
  - FPGAs – Field Programmable Gate Arrays
- FPGA – a chip you can program yourself
  - an IC foundry produces FPGAs with some connections missing
  - after design and simulation, special software is used to produce a string of bits describing the extra connections required to make the design – the configuration file
  - program the chip – make the necessary connections according to the configuration file

Introduction (cont'd)

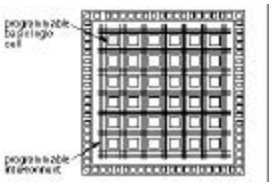
- No customization of any mask level
  - FPGA are manufactured as standard part in high volumes
- Ideal for prototyping or for low-volume production
- FPGA vendors do not need IC fabrication facility
  - Contract IC foundries to produce their parts
    - fabs cost hundreds of millions of dollars
  - Put their effort in architecture and software
    - much easier to make a profit by selling design software

FPGA Characteristics

- All have regular array of basic logic cells that are configured using a programming tech.
- Chip inputs and outputs use special I/O logic cells
- A programmable interconnect scheme forms the wiring between the two types of logic cells
- Designers use custom software, tailored for each programming technology and FPGA architecture to design and implement interconnections
- Types of programming technology
  - permanent programming (OTP – One Time Programmable)
  - Reprogrammable or erasable

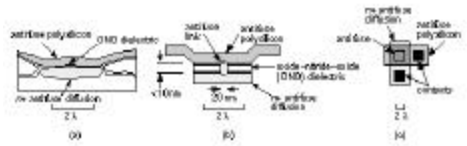
FPGA Internal Structure

- Top FPGA vendors in 2002 are Xilinx Inc. and Altera Corporation
- Basic internal structure
  - PLB – Programmable Logic Blocks
  - PI – Programmable Interconnect
- Current trends: include RAM and/or a fixed microprocessor core



Antifuse

- Antifuse
  - normally it is an open circuit until forcing a programming current through it
  - Actel calls its antifuse a programmable low-impedance circuit element (**PLICE**)
  - OTP technology



Antifuse (cont'd)

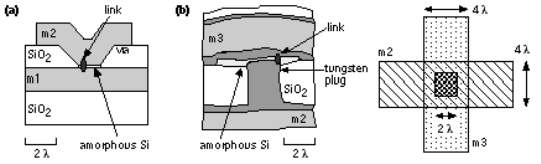
- Programming current controls the antifuse resistance (typically for 5mA it is 500 Ohms)
  - reduce resistance by increasing the current
- Design Steps
  - design entry + simulation until the design is correct
  - plug the chip into a socket on a special programming box, called Activator (provides programming voltage)
  - PC downloads the configuration file instruction the Activator which antifuses to blow
  - Remove the chip from the Activator
- In-system programming (ISP) – possibility to program the chip after it has been assembled on the PCB

Antifuse (cont'd)

- Actel antifuse technology uses modified CMOS process
  - double metal, single poly typically includes 12 masks
  - Actel process requires an additional 3 masks
- Actel A1010 – 112,000 antifuses, Actel A1020 – 186, 000 antifuses, …
- Programming time: 5 – 10 minutes

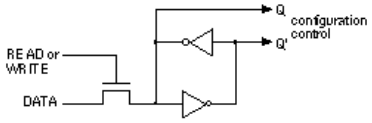
Metal-metal antifuse

- QuickLogic metal-metal antifuse
  - connections are direct to metal wiring layers
    - connections from poly-diffusion antifuse to wiring layers require extra space and create additional parasitics
  - easier to use larger programming currents to



Static RAM Programming

- Xilinx SRAM configuration cell
  - outputs Q and Q' are connected to the gates of pass transistors or transmission gates
  - cell is programmed using the WRITE and DATA lines

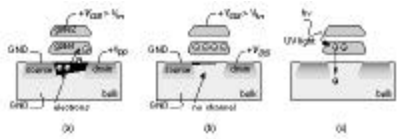


Static RAM Programming (cont'd)

- Advantages
  - reuse chip during prototyping
  - use ISP
  - possibility of upgrades
  - reconfigurable systems – change the system on the fly
- Disadvantage
  - keep the power supplied to the FPGA for SRAM to retain the connection information
  - alternatively, load the configuration from the permanently programmed memory (PROM) every time the system is turned on
  - increased area: SRAM + switches driven by SRAM cells

EPROM Technology

- EPROM - Electrically Programmable Read-only Memory
  - EPROM programmable, UV-erasable
  - E. g., Altera MAX 5000 EPLDs and Xilinx EPLDs



a) With a high (> 12 V) programming voltage, V_{PP} , applied to the drain, electrons gain enough energy to "jump" onto the floating gate (gate1). (b) Electrons stuck on gate1 raise the threshold voltage so that the transistor is always off for normal operating voltages.
(c) Ultraviolet light provides enough energy for the electrons stuck on gate1 to "jump" back to the bulk, allowing the transistor to operate normally.

EEPROM Technology

- EEPROM – Electrically Erasable Programmable Read-only Memory
  - Electrically programmable, UV-erasable
  - Electric field is used to remove electrons form the floating gate
- Advantages
  - faster than using a UV lamp
  - chips do not have to be removed from the system
  - if the system contains circuits to generate both program and erase voltages, it may use ISP

Specifications

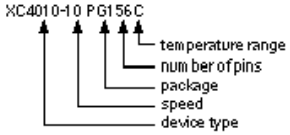
- FPGA manufacturers are continually improving their products in order to increase performance and reduce price
- Eg. Actel ACT 1
  - Actel ACT 1 A1010/A1020 – used 2um process
  - Actel ACT 1 A1010A/A1020A – used 1.2um process
  - Actel ACT 1 A1020B – used 1.0um process, die revision
- Parts with identical part numbers can have different performance
  - when different foundries produce the same parts

PREP Benchmarks

- Programmable Electronics Performance Company
  http://www.prep.org
  - non-profit organization that developed a series of benchmarks for FPGAs
- PREP 1.3
  1. An 8-bit datapath consisting of 4:1 MUX, register, and shift-register
  2. An 8-bit timer–counter consisting of two registers, a 4:1 MUX, a counter and a comparator
  3. A small state machine (8 states, 8 inputs, and 8 outputs)
  4. A larger state machine (16 states, 8 inputs, and 8 outputs)
  5. An ALU consisting of a 4 ∞ 4 multiplier, an 8-bit adder, and an 8-bit register
  6. A 16-bit accumulator
  7. A 16-bit counter with synchronous load and enable
  8. A 16-bit prescaled counter with load and enable
  9. A 16-bit address decoder

FPGA Economics

- FPGA vendors offer a wide variety of packing, speed, and qualification (military, industrial, or commercial) options in each family
- Xilinx part-naming convention



FPGA Pricing

- Xilinx XC3000 series options from 1992
  - Five different size parts: XC30{20, 30, 42, 64, 90}
  - Three different speed grades or bins: {50, 70, 100}
  - Ten different packages: {PC68, PC84, PG84, PQ100, CQ100, PP132, PG132, CQ184, PP175, PG175}
  - Four application ranges or qualification types: {C, I, M, B}
- 1992 base Xilinx XC3000 FPGA prices
  - XC3020-50PC68C $26.00
  - XC3030-50PC44C $34.20
  - XC3042-50PC84C $52.00
  - XC3064-50PC84C $87.00
  - XC3090-50PC84C $133.30

Summary

- FPGA programming technologies
  - antifuse
  - SRAM
  - EPROM technologies
- Key elements
  - The programming technology
  - The basic logic cells
  - The I/O logic cells
  - Programmable interconnect
  - Software to design and program the FPGA

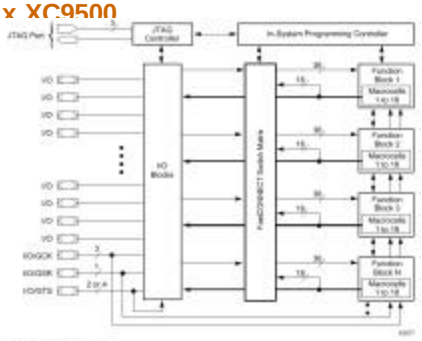
Advanced FPGAs

- Xilinx XC9500
- Xilinx Virtex-II
- Altera Stratix

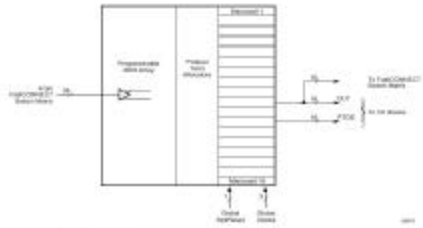
Xilinx XC9500

- Selected features
  - High-performance
    - 5 ns pin-to-pin logic delays on all pins
  - Large density range - 36 to 288 macrocells with 800 to 6,400 usable gates
  - 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
  - Programmable power reduction mode in each macrocell
  - High-drive 24 mA outputs
  - 3.3 V or 5 V I/O capability
  - Advanced CMOS 5V FastFLASH technology
  - Supports parallel programming of multiple XC9500 devices

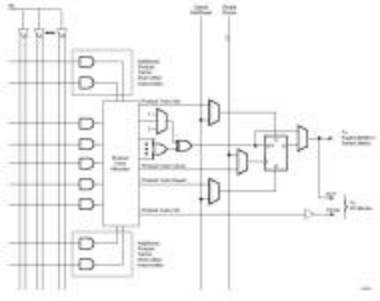
Xilinx XC9500



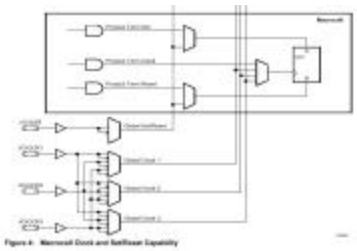
Xilinx XC9500 Function Block



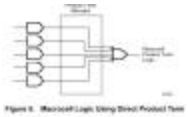
Xilinx XC9500 Macrocell

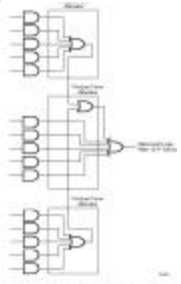


Xilinx XC9500 Macrocell Clock Set/Reset Cap.

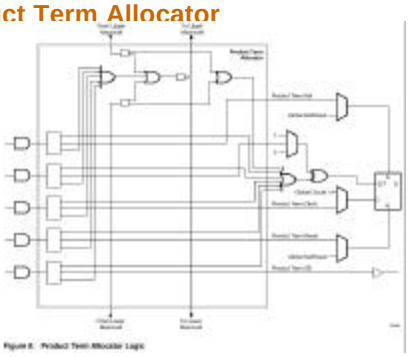


Product Term Allocator

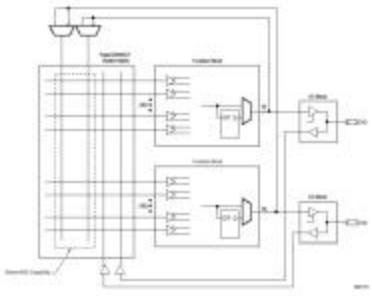




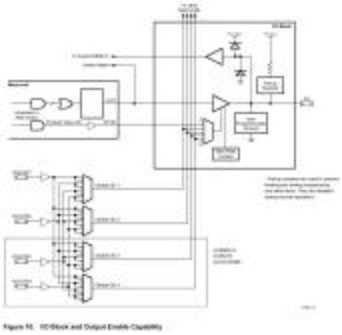
Product Term Allocator



FastCONNECT Switch Matrix



IO Block



Xilinx Virtex-II

- Selected features
  - 40K – 8M gates
  - 420 MHz internal clock speed
  - 840 Mb/s IO data
  - Arithmetic functions
    - dedicated 18x18 multipliers
    - fast look-ahead carry chains
  - Flexible logic resources
    - up to 93,184 registers/latches with Clock Enable
    - up to 93,184 LUTs or cascadable 16-bit registers
    - wide Muxes
    - internal 3-state bussing
  - …

Xilinx Virtex-II (cont'd)

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18-Kbit storage elements of True Dual-Port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse and fine-grained clock phase shifting.

Xilinx Virtex-II (cont'd)

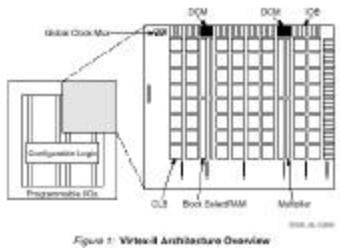


Figure 1: Virtex-II Architecture Overview

Altera Stratix PLD (cont'd)

- New high-performance architecture built for block-based design methodology
- Based on an industry-leading 1.5-V, 0.13-µm, all-layer-copper process
- System-Level Features
  - Up to 114,140 logic elements (LEs)
  - Up to 10 Mbits embedded memory and 12 terabits per second memory bandwidth
  - Up to 28 optimized digital signal processing (DSP) blocks
  - Up to 116 high-speed differential I/O channels with up to 80 channels optimized for 840-Mbps operation
  - Up to 12 phase-locked loops (PLLs) supporting 40 different clock domains
  - On-chip termination for differential and single-ended I/O standards that improves signal integrity and simplifies board layout
  - Convenient remote system upgrade capability and configuration error recovery circuitry

Altera Stratix PLD